Constraint-Based Code Generation

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Outline

What is code generation?

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- Target-independent program representation $\rightarrow$ Optimized target-specific assembly code

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    - One of the oldest computer science problems

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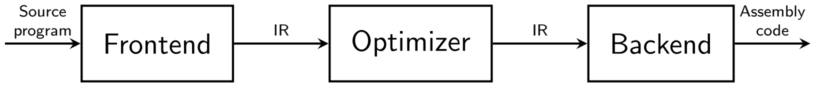
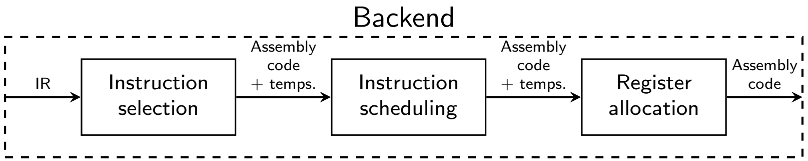
  - One of the oldest computer science problems
- Set of interdependent NP-complete problems
  - Traditionally solved using non-optimal heuristics
  - Phase ordering

Traditional compiler

Traditional compiler



Traditional compiler



Intermediate representation (IR)

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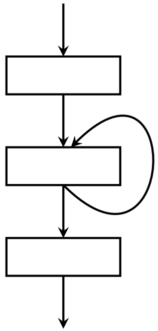
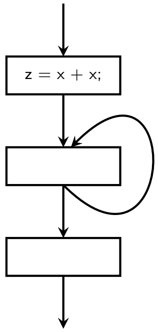


Control flow graph
(CFG), per function

Intermediate representation (IR)



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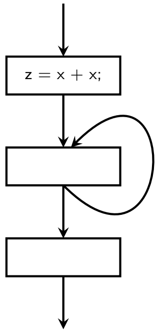

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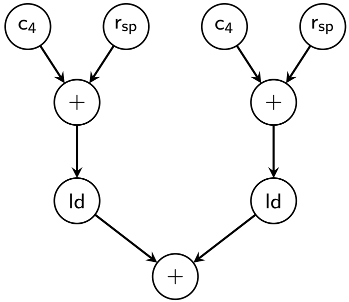
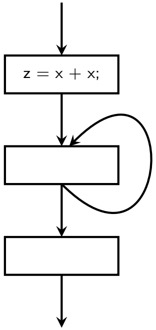


Expression tree, per block

Intermediate representation (IR)



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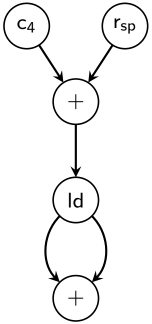

Directed acyclic graph (DAG)

From DAGs to assembly code

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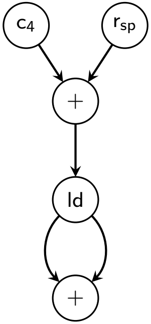

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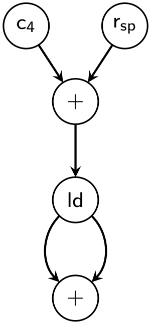

- Select which CPU instructions to use

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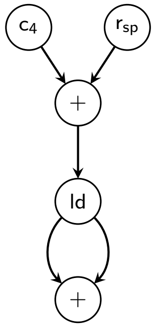

- Select which CPU instructions to use
  - Find covering with least cost

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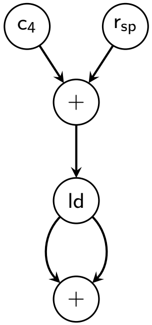

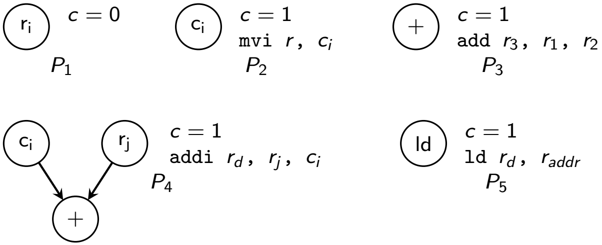

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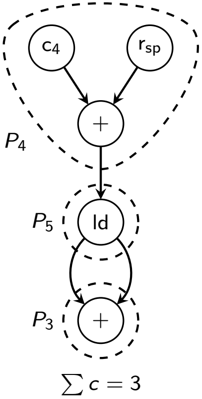

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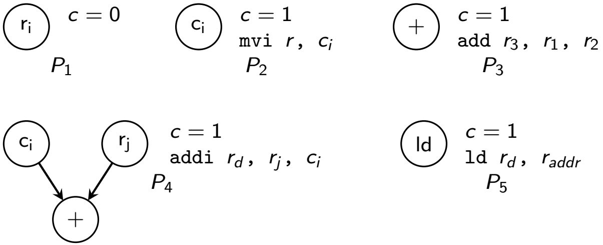

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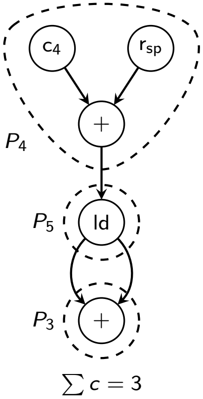

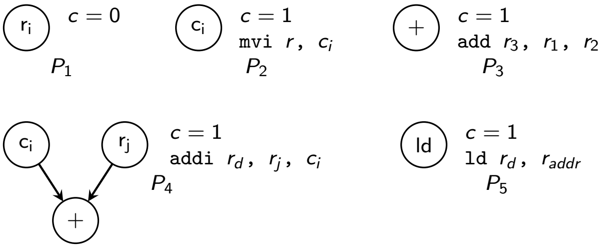

$\Longrightarrow$

```
addi t0, rsp, 4
ld t1, t0
add tz, t1, t1
```

From DAGs to assembly code

addi t_0, r_{sp}, 4
ld t_1, t_0
add t_z, t_1, t_1

From DAGs to assembly code

```
addi $t_0$, $r_{sp}$, 4
ld $t_1$, $t_0$
add $t_z$, $t_1$, $t_1$
```

- Schedule instructions

From DAGs to assembly code

```
addi $t_0$, $r_{sp}$, 4
ld $t_1$, $t_0$
add $t_z$, $t_1$, $t_1$
```

- Schedule instructions
- Assign temporaries to registers (or spill to memory)

From DAGs to assembly code

addi t_0, r_{sp}, 4
ld t_1, t_0
add t_z, t_1, t_1

addi r_0, r_{sp}, 4
ld r_1, r_0
add r_2, r_1, r_1

Requires 3 registers

- Schedule instructions
- Assign temporaries to registers (or spill to memory)

From DAGs to assembly code

```
addi $t_0$, $r_{sp}$, 4
ld $t_1$, $t_0$
add $t_z$, $t_1$, $t_1$
```

- Schedule instructions
- Assign temporaries to registers (or spill to memory)

```
addi $r_0$, $r_{sp}$, 4
ld $r_1$, $r_0$
add $r_2$, $r_1$, $r_1$
```

Requires 3 registers

```
addi $r_0$, $r_{sp}$, 4
ld $r_0$, $r_0$
add $r_0$, $r_0$, $r_0$
```

Requires only 1 register

Our Approach

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- Constraint programming

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    - Optimality

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*Given enough patience and money to burn while waiting

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    - Instruction selection - concepts / ideas

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- Constraint programming
  - Optimality*
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- Current status
  - Instruction selection - concepts / ideas
  - Instruction scheduling & register allocation - prototype + paper*

*Given enough patience and money to burn while waiting

**Constraint-based register allocation and instruction scheduling.* CP2012.

Instruction Selection

Which DAG node do we cover by which pattern?

Instruction Selection

Instruction Selection

1. Identify potential use of patterns in the DAG

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2. Find optimal covering

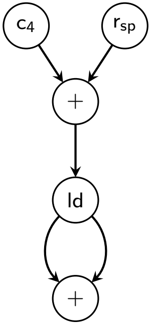
Instruction Selection

1. Identify potential use of patterns in the DAG
   - Use existing $O(n)$ techniques
2. Find optimal covering

Instruction Selection

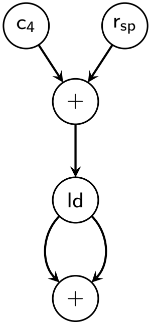
1. Identify potential use of patterns in the DAG
   - Use existing $O(n)$ techniques
2. Find optimal covering
   - Build and solve a constraint model

Instruction Selection



Instruction Selection

- Variables:



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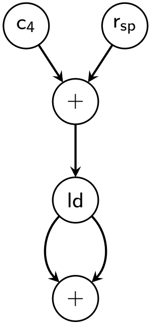
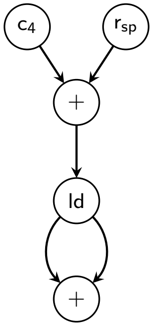


- Variables:
  - One integer variable for each DAG node to decide by which pattern instance is it covered

Instruction Selection



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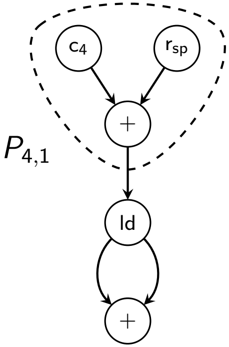

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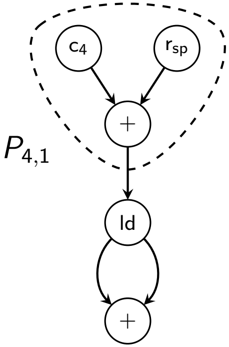

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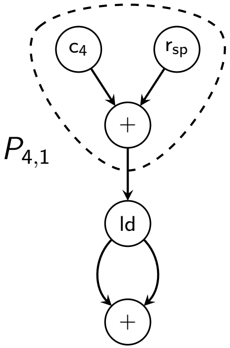
Instruction Selection



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$$D(\textcircled{c_4}) = P_{4,1} \iff D(\textcircled{+}) = P_{4,1}$$
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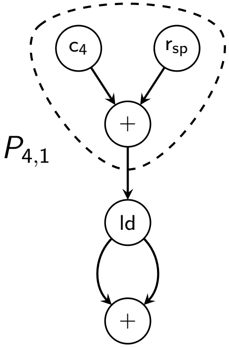

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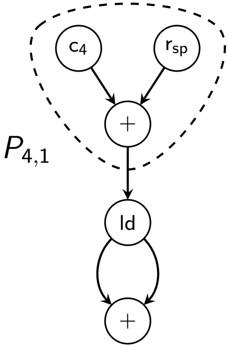
Instruction Selection



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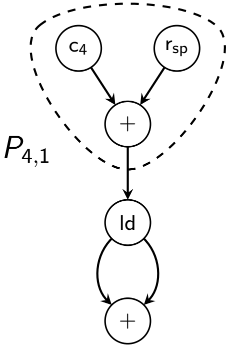
- Objective:

Instruction Selection



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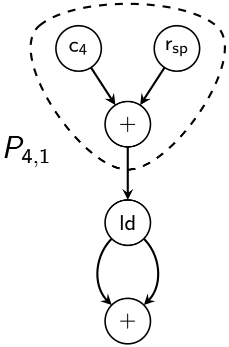
- Objective:

  $\min \sum_{p,i \in P_{p,i}} c_p B_{P_{p,i}}$

Instruction Selection



- Pattern restrictions can simply be added as constraints

Instruction Scheduling

in which cycle is each instruction issued?

Instruction Scheduling

- Classic scheduling model with:
  - precedences among instructions

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Instruction Scheduling

- Classic scheduling model with:
  - precedences among instructions

    if *i* defines a value used by *j*:

    i must be issued before *j*

  - resource constraints

    if *i* and *j* use the same functional unit:

    i and *j* must be issued in different cycles

Register Allocation

- Several problems
  - register assignment

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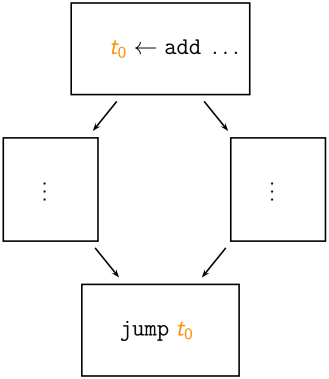
  - coalescing

Register Allocation

- Several problems
  - register assignment
  - spilling
  - coalescing
- Extra challenge: whole function

Liveness and Interference

- A temp is live while it might still be used:



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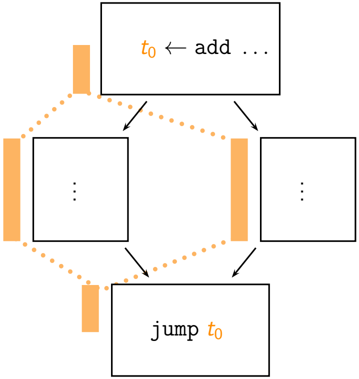

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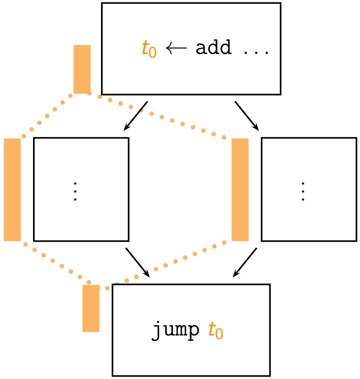

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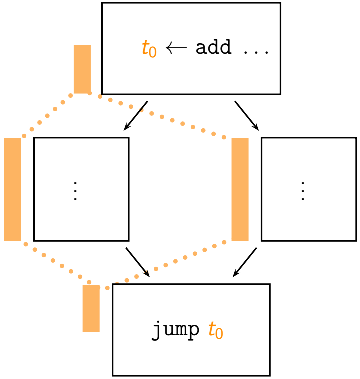

- Two temps interfere if they are live simultaneously
    - non-interfering temps can share registers

Linear Static Single Assignment Form (LSSA)

- t_0 is *global*: live in multiple blocks
- How to model interference of global temps?

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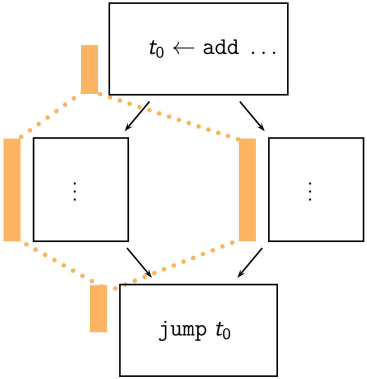

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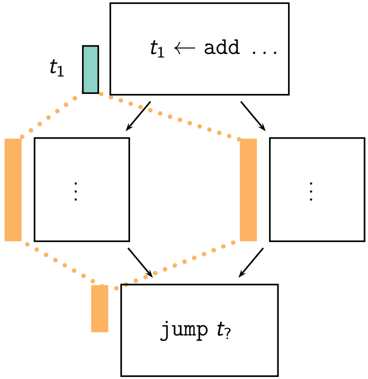

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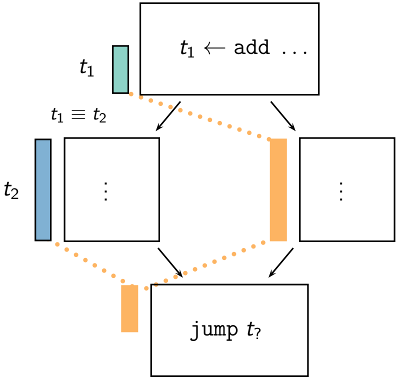

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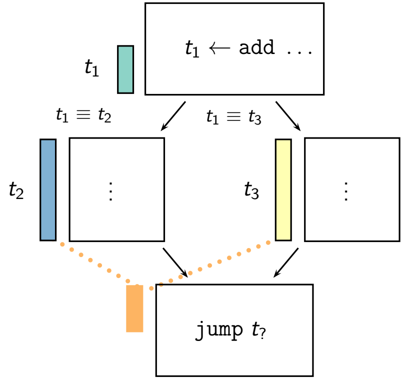

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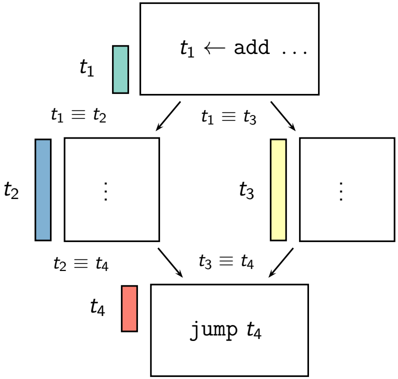

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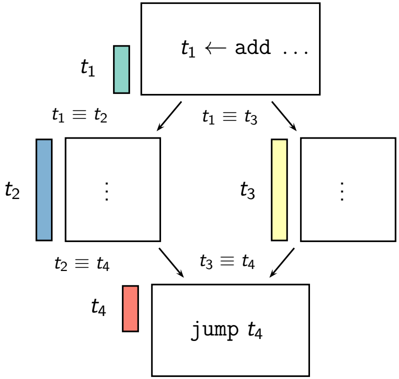

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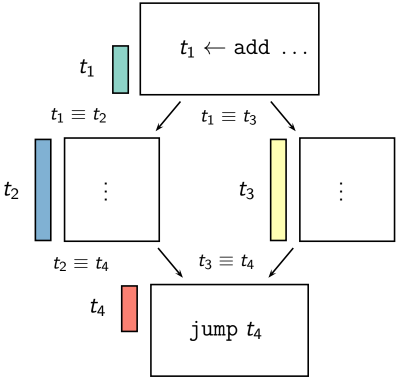

- Invariant: all temps are local $\rightarrow$ simple interference model

Register Assignment

to which register do we assign each temporary?

Register Assignment as Rectangle Packing

Register Assignment

Rectangle Packing

Register Assignment as Rectangle Packing

Register Assignment	Rectangle Packing
temp live ranges	rectangles

Register Assignment as Rectangle Packing

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temp live ranges	rectangles
temp size	rectangle width

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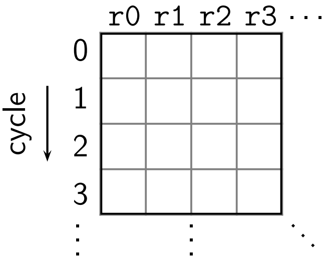

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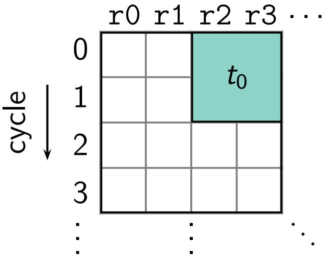

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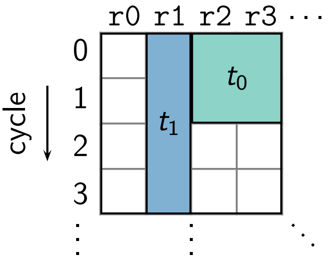

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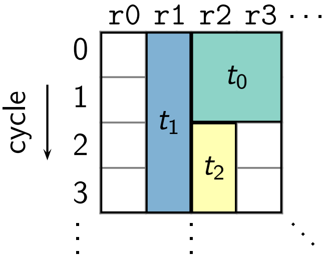
Register Assignment	Rectangle Packing
temp live ranges	rectangles
temp size	rectangle width
interfering temps cannot share registers	rectangles cannot overlap

$\rightarrow$ based on (Pereira *et al.*, 2008)



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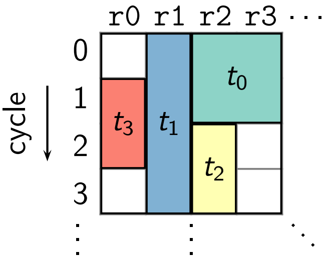

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Overcome Register Allocation Limitations

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- Work in progress . . .

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  3. if everything else fails, resort to greedy algorithms
     - *decent* polynomial solutions always available